

SN75LBC978 9-CHANNEL DIFFERENTIAL TRANSCIVER

SLLS134F – APRIL 1992 – REVISED APRIL 2005

- **Nine Differential Channels for the Data and Control Paths of the Differential Small Computer Systems Interface (SCSI)**
- **Meets or Exceeds the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **Packaged in Shrink Small-Outline Package With 25-mil Terminal Pitch**
- **Designed to Operate at 10 Million Transfers Per Second**
- **Low Disabled Supply Current
1.4 mA Typ**
- **Thermal Shutdown Protection**
- **Power-Up/Power-Down Glitch Protection**
- **Positive and Negative Output-Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**

description

The SN75LBC978 is a nine-channel differential transceiver based on the 75LBC176 LinASIC™ cell. Use of TI's LinBiCMOS™† process technology allows the power reduction necessary to integrate nine differential balanced transceivers†. On-chip enabling logic makes this device applicable for the data path (eight data bits plus parity) and the control path (nine bits) for the Small Computer Systems Interface (SCSI) standard. The WRAP function allows in-circuit testing and wired-OR channels for the BSY, RST, and SEL signals of the SCSI bus.

The SN75LBC978 is packaged in a shrink small-outline package (DL) with improved thermal characteristics using heat-sink terminals. This package is ideal for low-profile, space-restricted applications such as hard disk drives.

The switching speed of the SN75LBC978 is sufficient to transfer data over the data bus at 10 million transfers per second. Each of the nine identical channels conforms to the requirements of the ANSI RS-485 and ISO 8482:1987(E) standards referenced by ANSI X3.131-1993 (SCSI-2) and the proposed SCSI-3 standards.

The SN75LBC978 is characterized for operation from 0°C to 70°C.

DL PACKAGE
(TOP VIEW)

| | | | |
|-----------------|----|----|-----------------|
| NC | 1 | 56 | NC |
| WRAP2 | 2 | 55 | NC |
| WRAP1 | 3 | 54 | CE |
| 1A | 4 | 53 | 9B+ |
| 1DE/RE | 5 | 52 | 9B- |
| 2A | 6 | 51 | 8B+ |
| 2DE/RE | 7 | 50 | 8B- |
| 3A | 8 | 49 | 7B+ |
| 3DE/RE | 9 | 48 | 7B- |
| 4A | 10 | 47 | 6B+ |
| 4DE/RE | 11 | 46 | 6B- |
| V _{CC} | 12 | 45 | V _{CC} |
| GND | 13 | 44 | GND |
| GND | 14 | 43 | GND |
| GND | 15 | 42 | GND |
| GND | 16 | 41 | GND |
| GND | 17 | 40 | GND |
| V _{CC} | 18 | 39 | V _{CC} |
| 5A | 19 | 38 | 5B+ |
| 5DE/RE | 20 | 37 | 5B- |
| 6A | 21 | 36 | 4B+ |
| 6DE/RE | 22 | 35 | 4B- |
| 7A | 23 | 34 | 3B+ |
| 7DE/RE | 24 | 33 | 3B- |
| 8A | 25 | 32 | 2B+ |
| 8DE/RE | 26 | 31 | 2B- |
| 9A | 27 | 30 | 1B+ |
| 9DE/RE | 28 | 29 | 1B- |

Pins 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

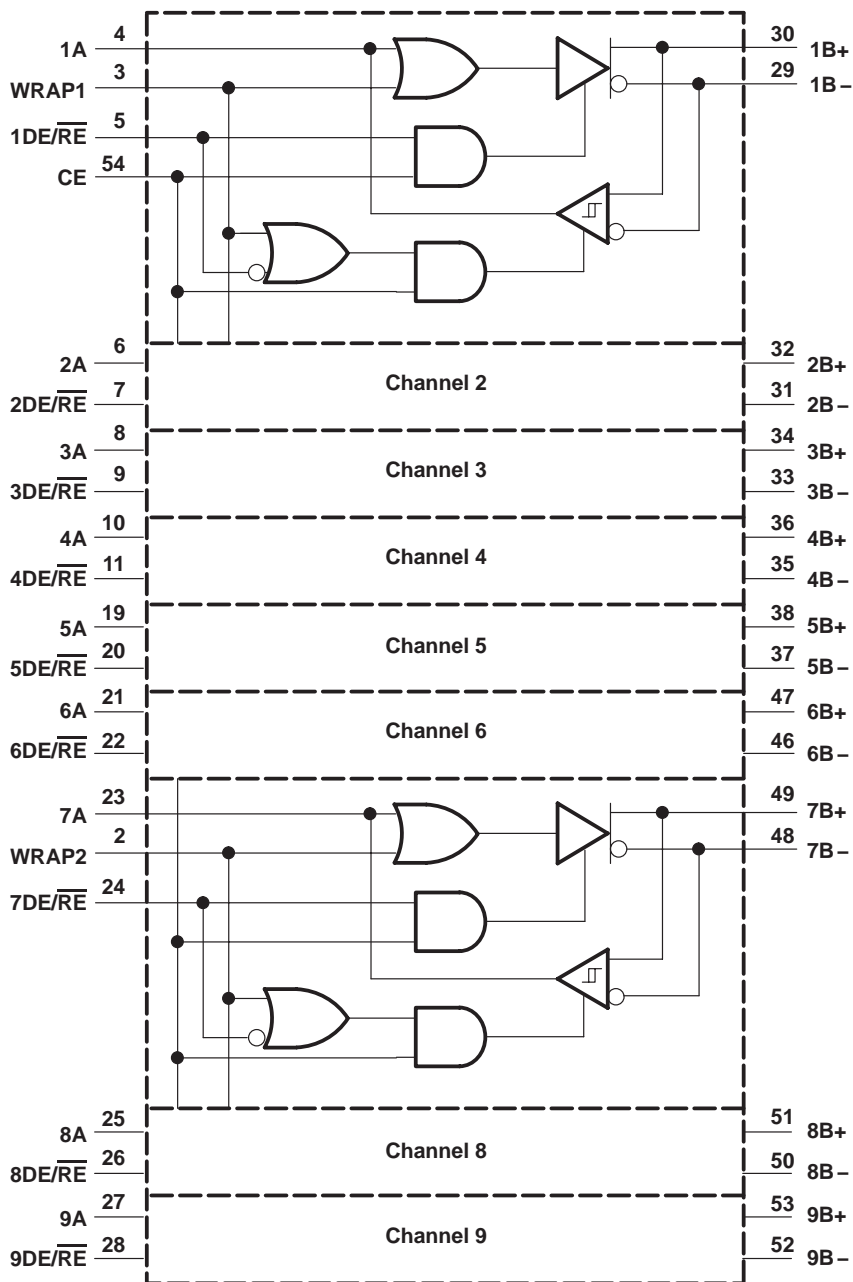
† Patent Pending

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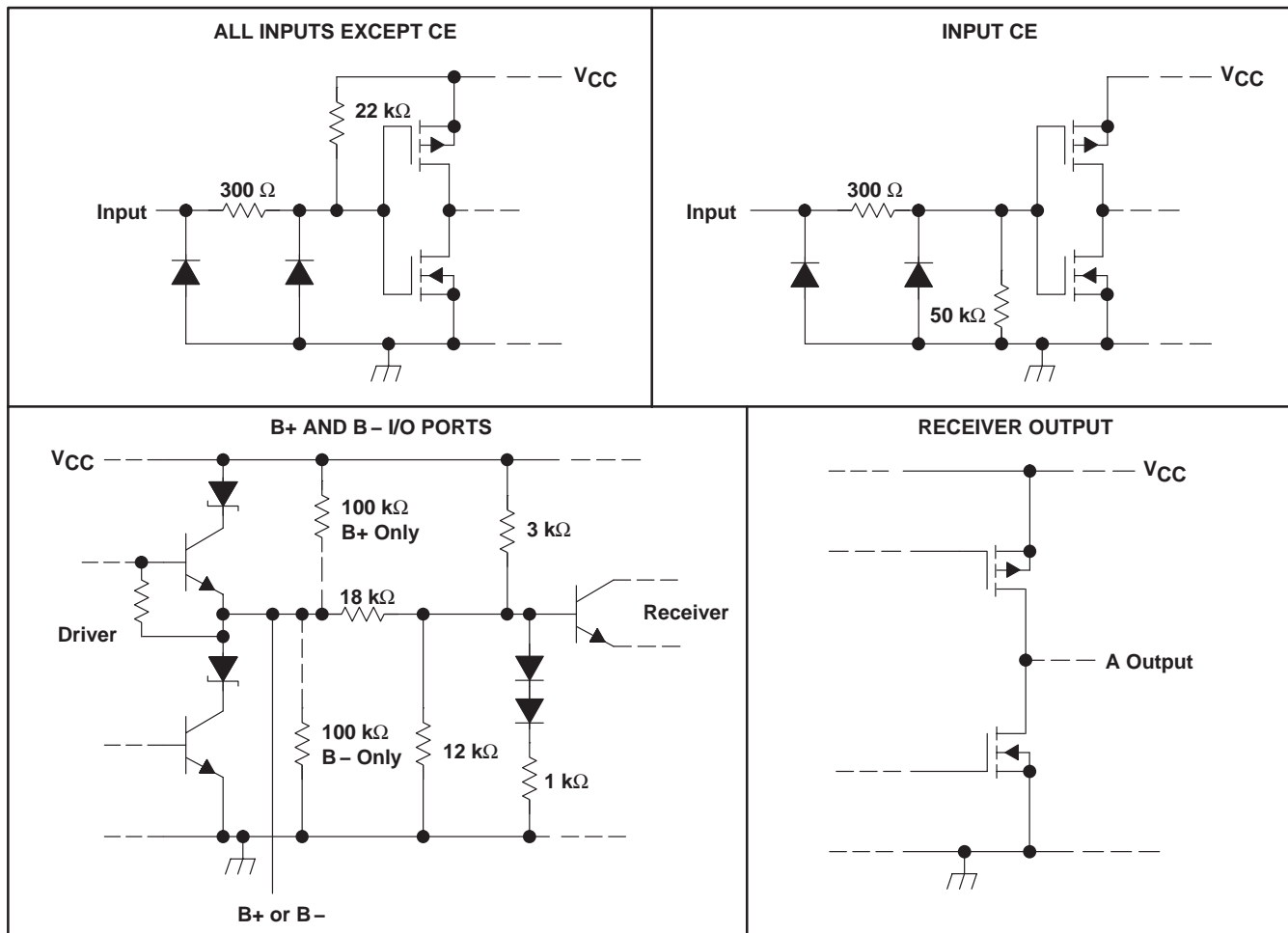
SN75LBC978 9-CHANNEL DIFFERENTIAL TRANSCIEVER

SLLS134F – APRIL 1992 – REVISED APRIL 2005

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|--------------------|
| Supply voltage range, V_{CC} (see Note 1) | –0.3 V to 7 V |
| Bus voltage range | –10 V to 15 V |
| Data I/O and control (A-side) voltage range | –0.3 V to 7 V |
| Receiver output current, I_O | ± 24 mA |
| Continuous power dissipation | internally limited |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are dc and with respect to GND.

SN75LBC978

9-CHANNEL DIFFERENTIAL TRANSCEIVER

SLLS134F – APRIL 1992 – REVISED APRIL 2005

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|----------------------|------|-----|------|------|
| Supply voltage, V_{CC} | | 4.75 | 5 | 5.25 | V |
| Voltage at any bus terminal (separately or common-mode), V_O , V_I , or V_{IC} | B+ or B- | 12 | | | V |
| | | -7 | | | |
| High-level input voltage, V_{IH} | All except B+ and B- | 2 | | | V |
| Low-level input voltage, V_{IL} | All except B+ and B- | | | 0.8 | V |
| High-level output current, I_{OH} | B+ or B- | | | -60 | mA |
| | A | | | -8 | mA |
| Low-level output current, I_{OL} | B+ or B- | | | 60 | mA |
| | A | | | 8 | mA |
| Operating free-air temperature, T_A | | 0 | | 70 | °C |

device electrical characteristics over recommended ranges of operating conditions

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-----------|-------------------------------|------------------------------------|--|-------------------------|------|------|---------------|
| I_{IH} | High-level input current | A, WRAP, $\overline{DE/RE}$ | See Figure 1 | $V_{IH} = 2\text{ V}$ | | -200 | μA |
| | | CE | | | | 100 | μA |
| I_{IL} | Low-level input current | A, WRAP, $\overline{DE/RE}$ | See Figure 1 | $V_{IL} = 0.8\text{ V}$ | | -200 | μA |
| | | CE | | | | 100 | μA |
| I_{CC} | Supply current | All drivers and receivers disabled | CE at 0 V | | 1.4 | 3 | mA |
| | | All receivers enabled | No load, CE at 5 V, $V_{ID} = 5\text{ V}$, WRAP and $\overline{DE/RE}$ at 0 V | | 29 | 45 | mA |
| | | All drivers enabled | No load, CE and $\overline{DE/RE}$ at 5 V, WRAP at 0 V | | 7 | 10 | mA |
| C_O | Bus port output capacitance | B+ or B- | | | 19 | | pF |
| C_{pd} | Power dissipation capacitance | One driver | | | 460 | | pF |
| | | One receiver | | | 40 | | pF |

driver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------|-------------------------------------|--|--|-----|-----|-----------|------|
| $ V_{OD} $ | Differential output voltage | $V_{test} = -7\text{ V to }12\text{ V}$, See Figure 2 | | 1 | 2 | | V |
| I_{OS} | Output short-circuit current | See Figure 3 | | | | ± 250 | mA |
| I_{OZ} | High-impedance-state output current | See receiver input current | | | | | |



receiver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted) (see Figure 3)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|--|---|---|------|------|------|
| V _{OH} | High-level output voltage | V _{ID} = 200 mV, I _{OH} = -8 mA | 2.5 | | | V |
| V _{OL} | Low-level output voltage | V _{ID} = -200 mV, I _{OL} = 8 mA | | | 0.8 | V |
| V _{IT+} | Differential-input high-level threshold voltage | I _{OH} = -8 mA | | | 0.2 | V |
| V _{IT-} | Differential-input low-level threshold voltage | I _{OL} = 8 mA | -0.2 | | | V |
| V _{hys} | Receiver input hysteresis voltage (V _{IT+} - V _{IT-}) | | | 45 | | mV |
| I _I | Receiver input current | B+ and B- | V _I = 12 V, V _{CC} = 5 V, Other input at 0 V | 0.7 | 1 | mA |
| | | | V _I = 12 V, V _{CC} = 0 V, Other input at 0 V | 0.8 | 1 | mA |
| | | | V _I = -7 V, V _{CC} = 5 V, Other input at 0 V | -0.5 | -0.8 | mA |
| | | | V _I = -7 V, V _{CC} = 0 V, Other input at 0 V | -0.4 | -0.8 | mA |
| I _{OZ} | High-impedance-state output current | V _O = GND | | | -200 | μA |
| | | V _O = V _{CC} | | | 50 | |

driver switching characteristics over recommended ranges of operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|----------------------|---|---|------|------|------|------|
| t _{d(OD)} | Differential delay time, high- to low-level output (t _{d(ODH)}) or low- to high-level output (t _{d(ODL)}) | See Figure 4 | 11.8 | | 26.4 | ns |
| | | V _{CC} = 5 V, T _A = 25°C, See Figure 4 | 14 | 18 | 22 | |
| | | V _{CC} = 5 V, T _A = 70°C, See Figure 4 | 18 | 22 | 26 | |
| t _{sk(lim)} | Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices | | | | 15 | ns |
| | | V _{CC} = 5 V, See Note 2 | | | 8 | |
| t _{sk(p)} | Pulse skew (t _{d(ODL)} - t _{d(ODH)}) | | | 0 | 6 | ns |
| t _t | Transition time (t _r or t _f) | See Figure 4 | | 10 | | ns |

receiver switching characteristics over recommended ranges of operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|----------------------|--|---|------|------|------|------|
| t _{pd} | Propagation delay time, high- to low-level output (t _{PHL}) or low- to high-level output (t _{PLH}) | See Figure 5 | 19.5 | | 30.7 | ns |
| | | V _{CC} = 5 V, T _A = 25°C, See Figure 5 | 20.2 | 24.7 | 29.2 | |
| | | V _{CC} = 5 V, T _A = 70°C, See Figure 5 | 21.1 | 25.6 | 30.1 | |
| t _{sk(lim)} | Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices | | | | 12 | ns |
| | | V _{CC} = 5 V, See Note 2 | | | 9 | |
| t _{sk(p)} | Pulse skew (t _{PHL} - t _{PLH}) | | | 2 | 6 | ns |
| t _t | Transition time (t _r or t _f) | See Figure 5 | | 3 | | ns |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ C_{pd} determines the no-load dynamic current consumption; I_S = C_{pd} · V_{CC} · f + I_{CC}.

NOTE 2: This specification applies to any 5°C band within the operating temperature range.

SN75LBC978 9-CHANNEL DIFFERENTIAL TRANSCIVER

SLLS134F – APRIL 1992 – REVISED APRIL 2005

transceiver switching characteristics over recommended ranges of operating conditions

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------|--|-----------------|-----|-----|------|
| $t_{en}(TXL)$ | Enable time, transmit-to-receive to low-level output | See Figure 6 | 80 | | ns |
| $t_{en}(TXH)$ | Enable time, transmit-to-receive to high-level output | | 80 | | ns |
| $t_{en}(RXL)$ | Enable time, receive-to-transmit to low-level output | | 150 | | ns |
| $t_{en}(RXH)$ | Enable time, receive-to-transmit to high-level output | | 150 | | ns |
| t_{su} | Setup time, WRAP1 or WRAP2 before active input(s) or output(s) | | 150 | | ns |

thermal characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|----------------------------|-----|-----|-----|------|
| $R_{\theta JA}$ | Junction-to-free-air thermal resistance | Board mounted, No air flow | | 50 | | °C/W |
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | | 12 | | °C/W |

PARAMETER MEASUREMENT INFORMATION

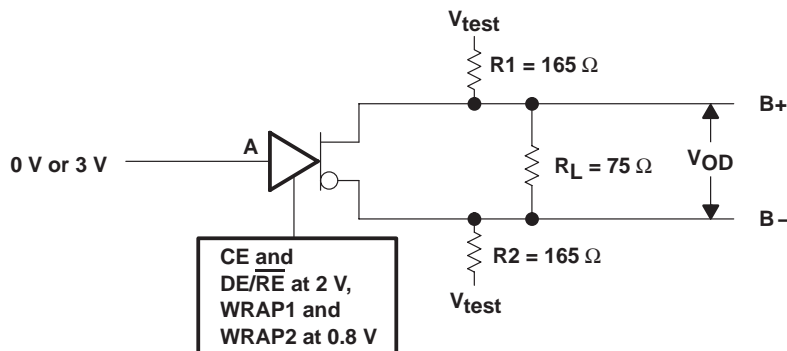
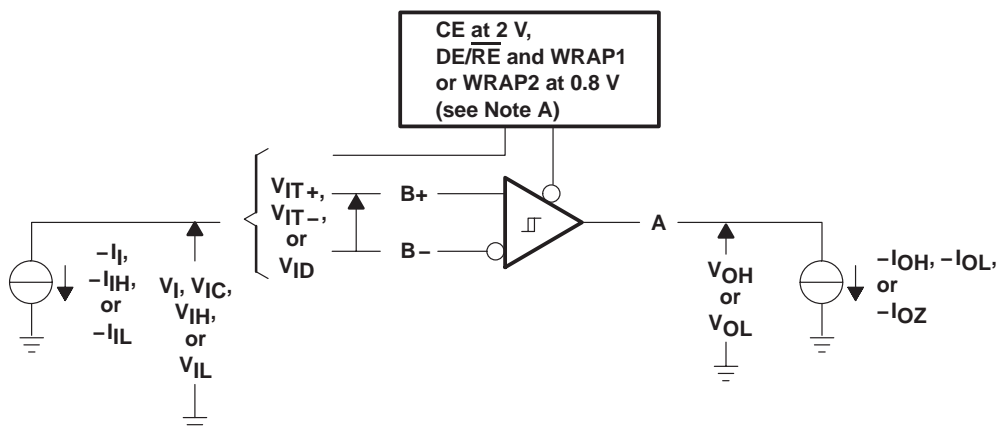


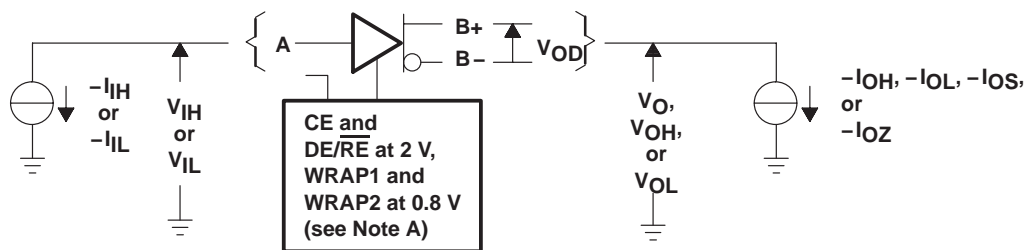
Figure 1. Driver V_{OD} Test Circuit



NOTE A: For the I_{OZ} measurement, CE is at 0.8 V.

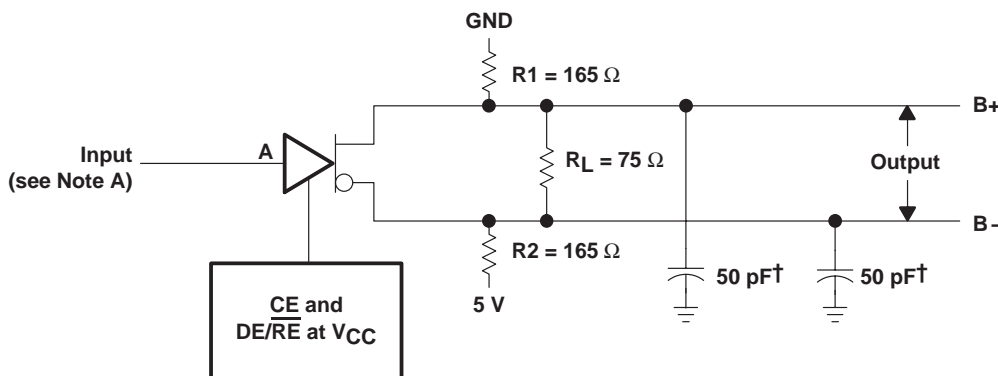
Figure 2. Receiver Test Circuit and Input Conditions

PARAMETER MEASUREMENT INFORMATION

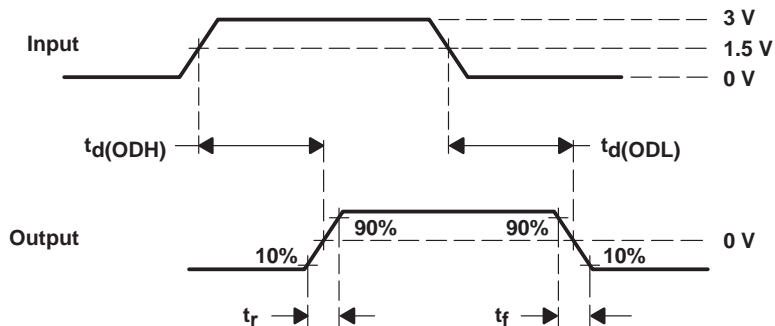


NOTE A: For the I_{OZ} test, the CE input is at 0.8 V.

Figure 3. Driver Test and Input Conditions



TEST CIRCUIT



VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

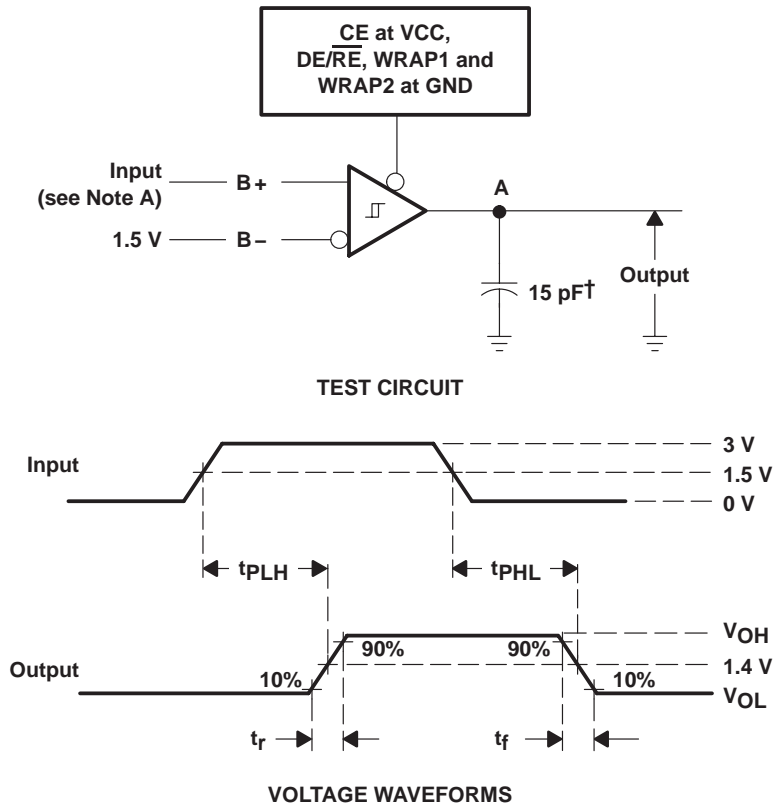
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and $t_f < 6$ ns, and $Z_O = 50 \Omega$.

Figure 4. Driver Propagation Delay Time Test Circuit and Waveforms

SN75LBC978 9-CHANNEL DIFFERENTIAL TRANSCIEVER

SLLS134F – APRIL 1992 – REVISED APRIL 2005

PARAMETER MEASUREMENT INFORMATION

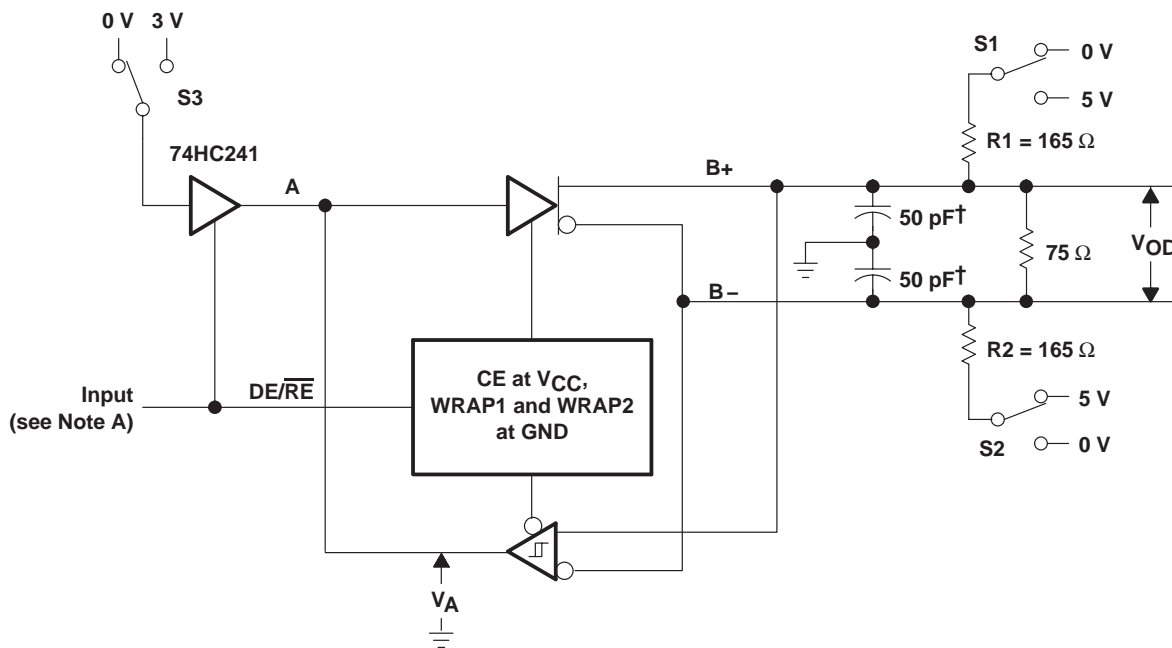


† Includes probe and jig capacitance.

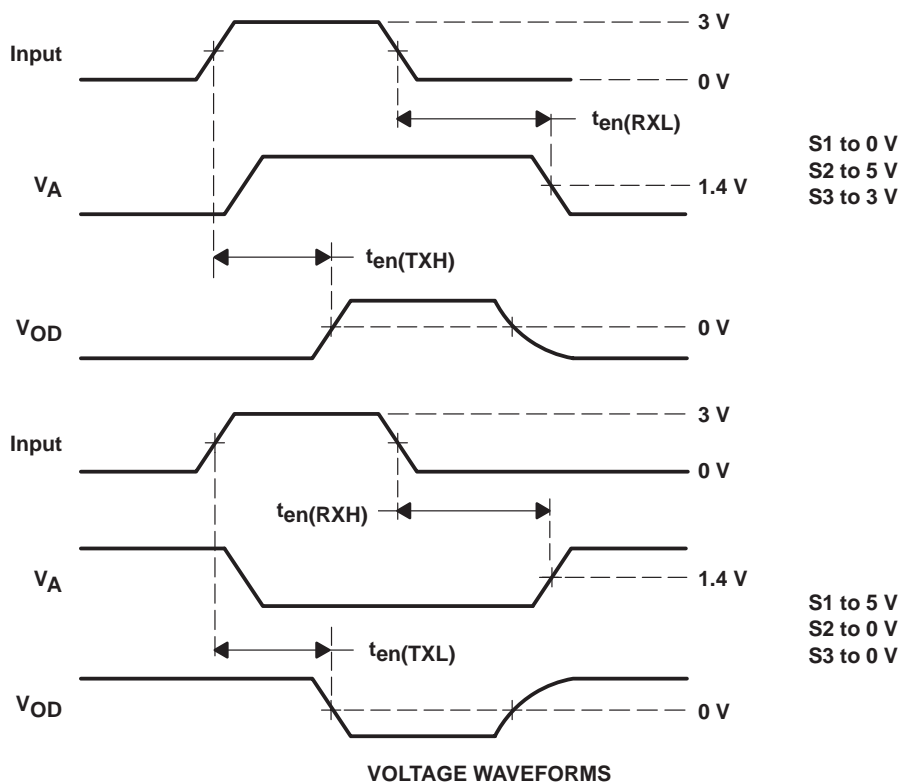
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 5. Receiver Propagation Delay Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and $t_f < 6$ ns, and $Z_O = 50 \Omega$.

Figure 6. Enable Time Test Circuit and Voltage Waveforms

SN75LBC978 9-CHANNEL DIFFERENTIAL TRANSCEIVER

SLLS134F – APRIL 1992 – REVISED APRIL 2005

TYPICAL CHARACTERISTICS

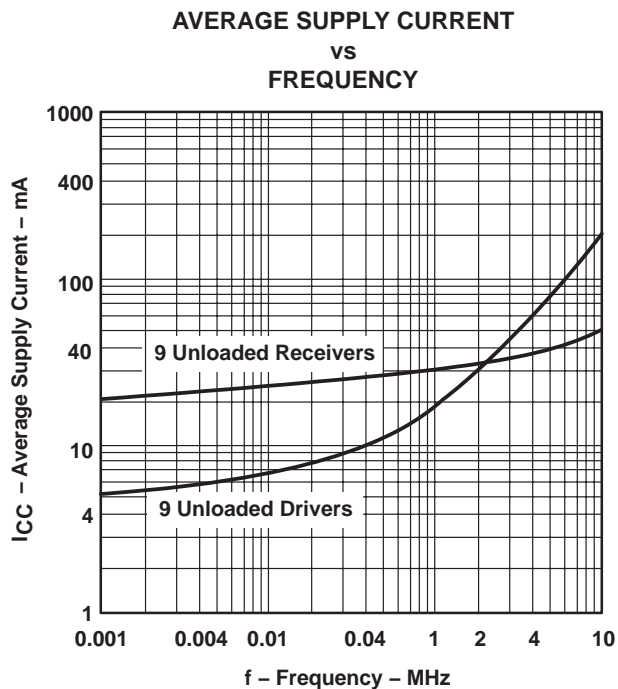


Figure 7

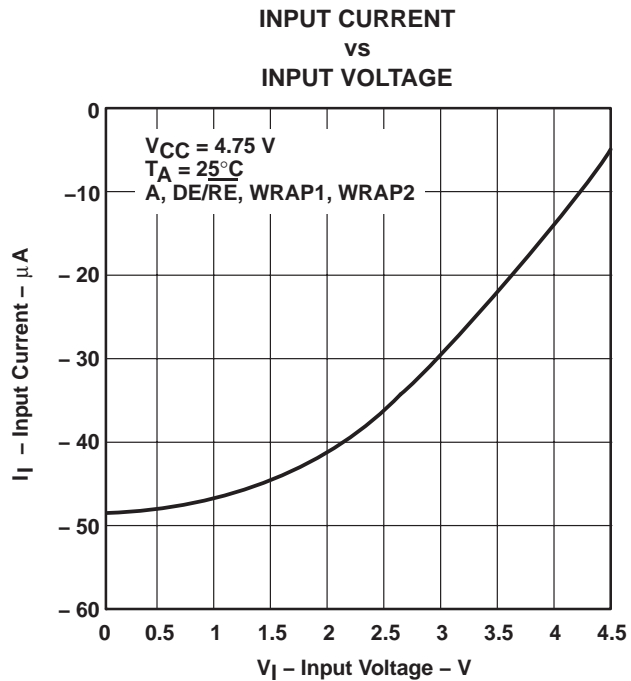


Figure 8

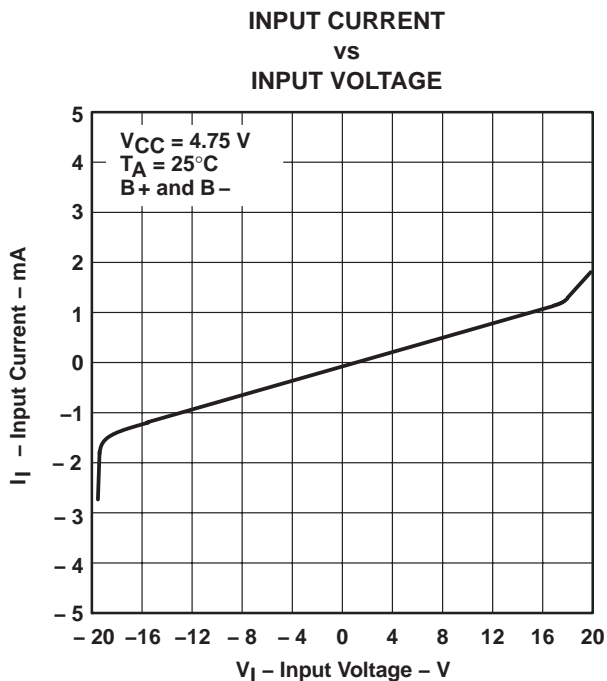
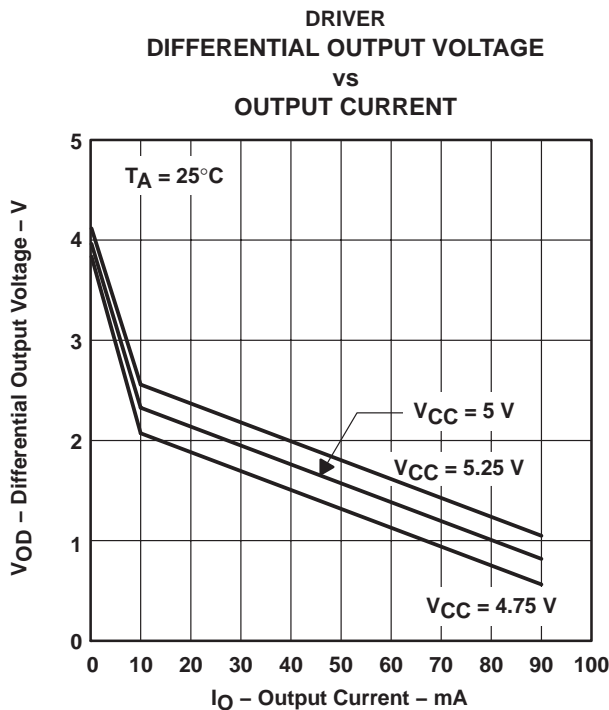
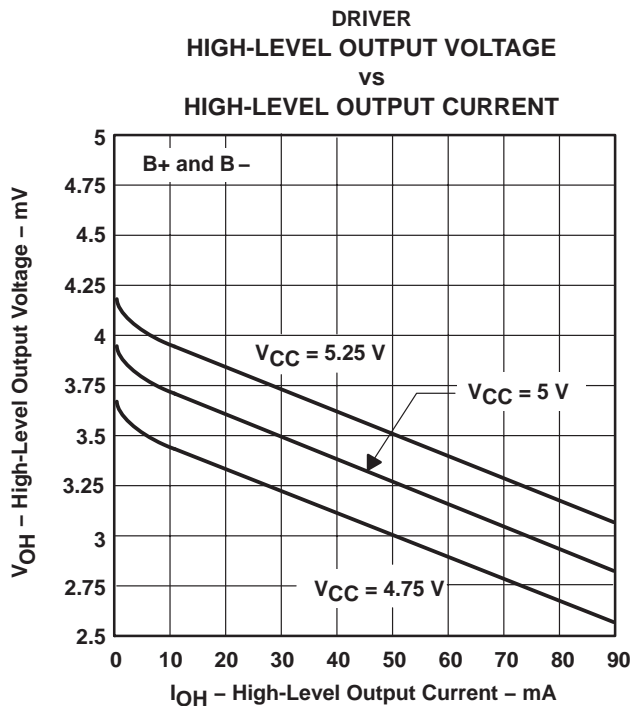
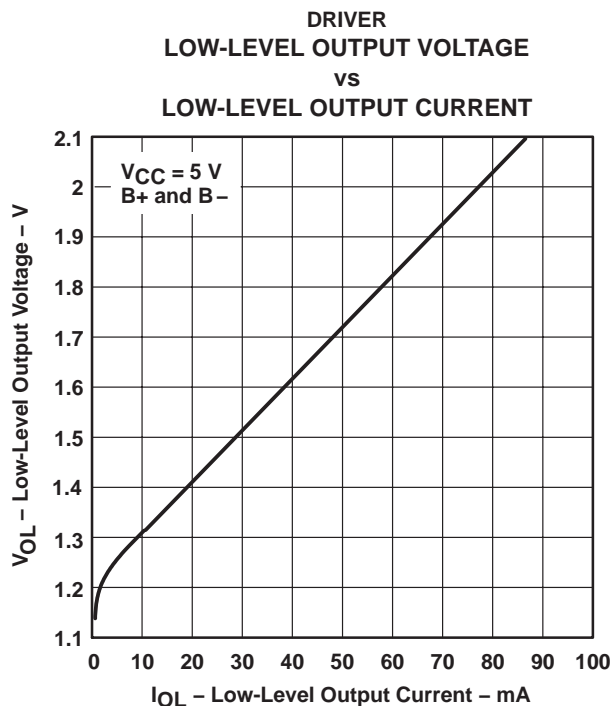


Figure 9

TYPICAL CHARACTERISTICS



SN75LBC978 9-CHANNEL DIFFERENTIAL TRANSCIEVER

SLLS134F – APRIL 1992 – REVISED APRIL 2005

TYPICAL CHARACTERISTICS

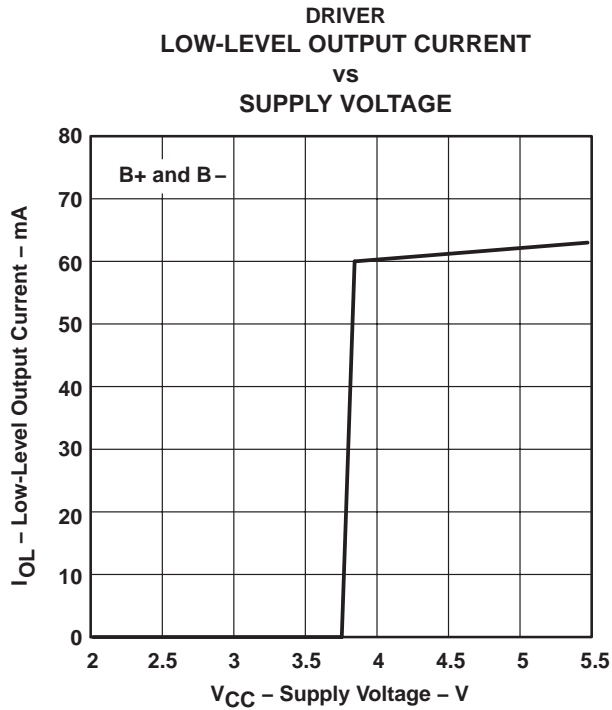


Figure 13

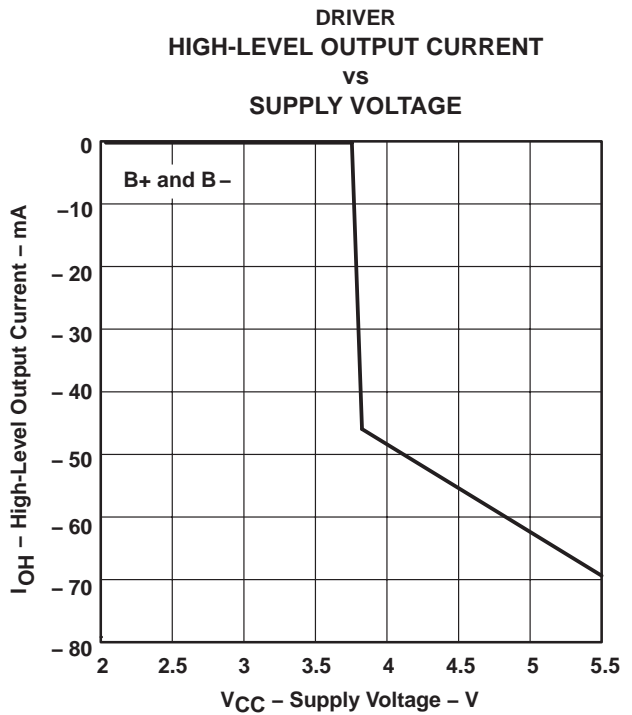


Figure 14

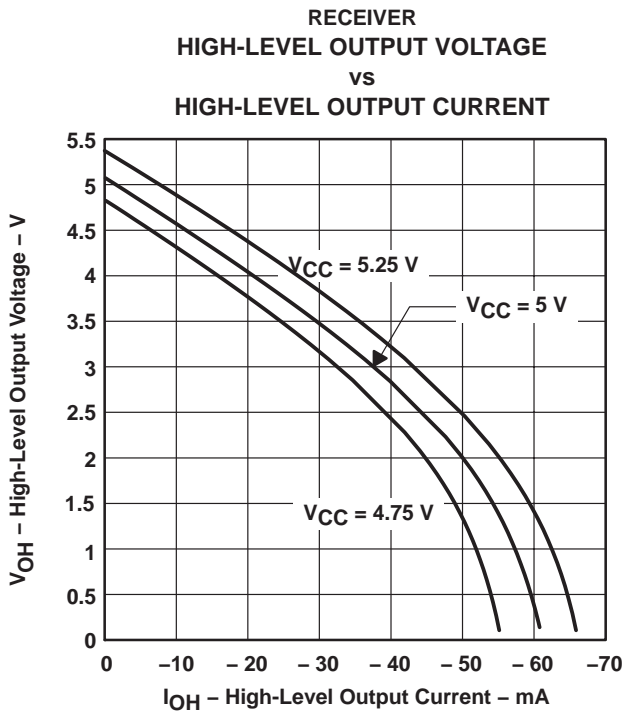


Figure 15

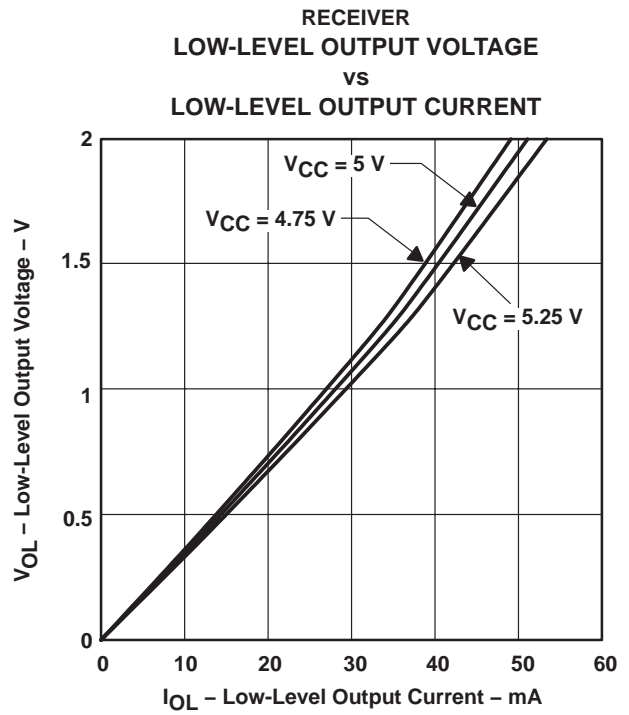


Figure 16

TYPICAL CHARACTERISTICS

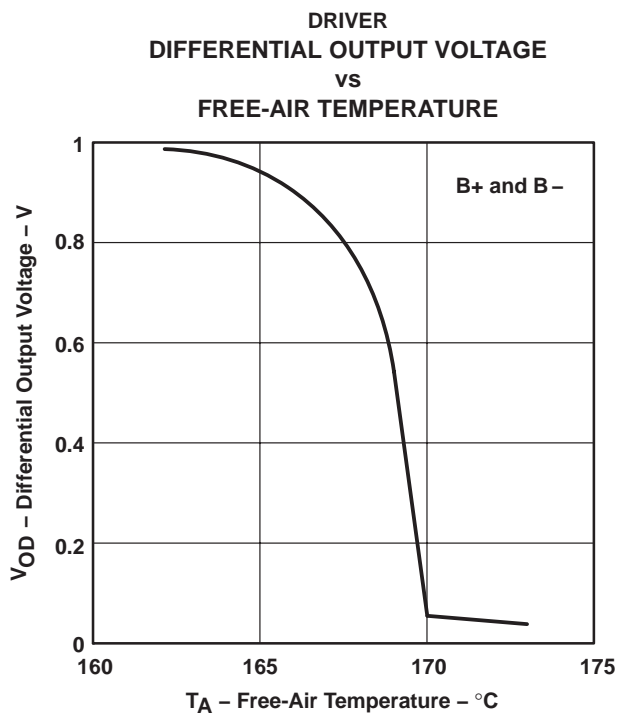


Figure 17

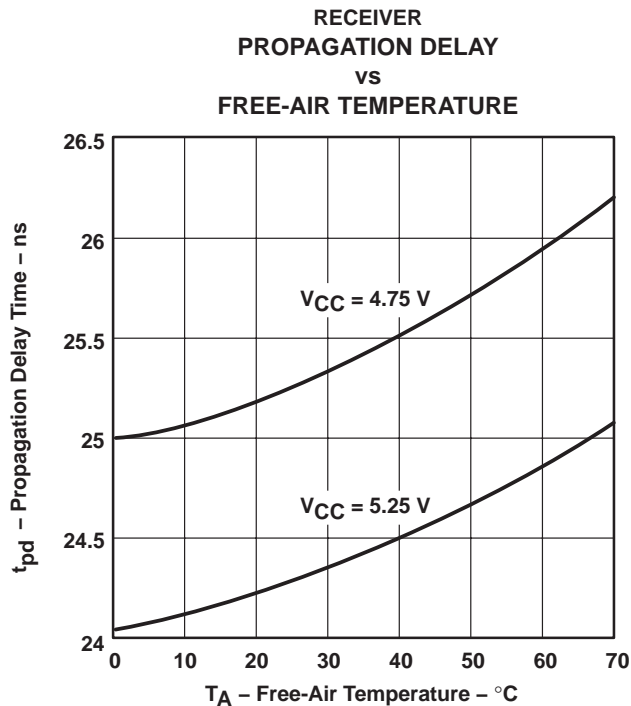


Figure 18

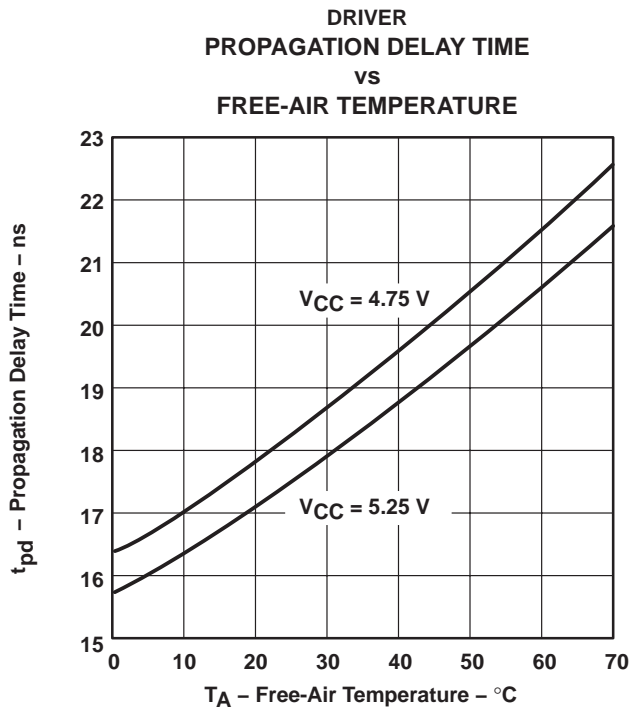


Figure 19

SN75LBC978 9-CHANNEL DIFFERENTIAL TRANSCEIVER

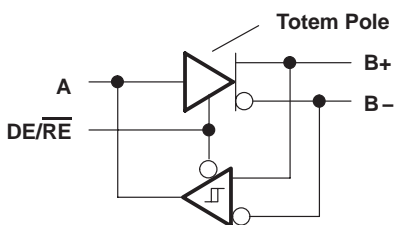
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APPLICATION INFORMATION

function tables

Table 1. Channel Configuration for Totem Pole Circuit

CE is high,
WRAP1 or WRAP2 is low



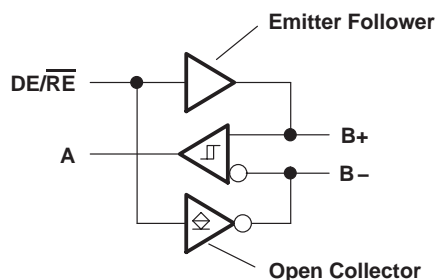
| INPUTS | | | | OUTPUTS | | |
|--------|---|-----|-----|---------|----|----|
| DE/RE | A | B+† | B-† | A | B+ | B- |
| L | X | L | H | L | Z | Z |
| L | X | H | L | H | Z | Z |
| H | L | X | X | Z | L | H |
| H | H | X | X | Z | H | L |

H = high level L = low level X = irrelevant Z = high impedance

† An H in this column represents a voltage 200 mV higher than the other bus input. An L represents a voltage 200 mV lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

Table 2. Channel Configuration for Emitter Follower Circuit

CE is high,
WRAP1 or WRAP2 is high



| INPUTS | | | OUTPUTS | | |
|--------|----|----|---------|----|----|
| DE/RE | B+ | B- | A | B+ | B- |
| L | L | H | L | Z | Z |
| L | H | L | H | Z | Z |
| H | X | X | H | H | L |
| H | X | X | H | H | L |

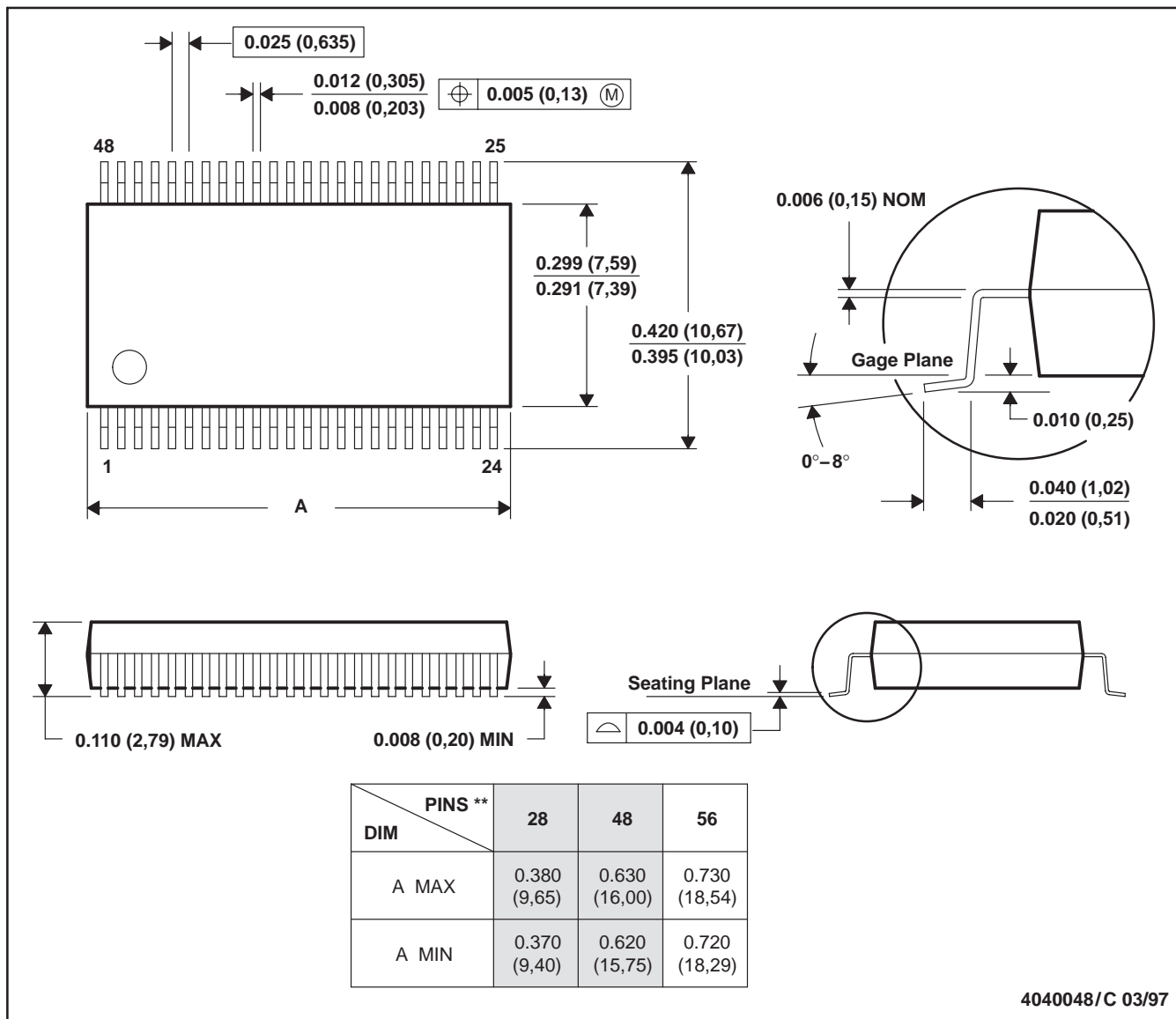
H = high level L = low level X = irrelevant Z = high impedance

MECHANICAL INFORMATION

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN75LBC978DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LBC978DLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LBC978DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LBC978DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75LBC978DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75LBC978DLR | SSOP | DL | 56 | 1000 | 346.0 | 346.0 | 49.0 |

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